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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,901	09/05/2003	Blake Little	65744/P011C1/10313161	1544

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EXAMINER	
JAWORSKI, FRANCIS J	

ART UNIT	PAPER NUMBER
3737	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,901	LITTLE ET AL.	
	Examiner	Art Unit	
	Jaworski Francis J.	3737	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

[Parenthesized claim numbers refer to the specific claim or claims under rejection by the immediately preceding argument.]

Claims 3-5, 13-15 are again rejected under 35 U.S.C. 102(b) as being anticipated by Pflugrath et al (US5722412) which teaches:

A pulse wave transmission system (col. 5 lines 7 – 31) which includes a Doppler function in ASIC 40, see discussion of the DSP ASIC 40 spanning col. 9 line 21 – col. 14 line 22 , in particular

col. 11 line 53 – col. 13 bottom which describes pulse Doppler processing.

Pflugrath et al is further characterizable as having a beamformer at DELAY-SUM 320 (see col. 7 line 11) and a transducer controller (TRANSMIT& TIMING CONTROL), a digital signal processor (DSP ASIC 40, see col. 9 lines 21 – 22), .a plurality of memories (32,42,52,54,408,420, 430, 502,530, 550 and a dual ported RAM implementation for the delay lines) with attendant I/O channels, power control 80, transducer array 10 and user interface 70. All ASIC functions of 20, 30, 40 and 50 may be combined within a single ASIC circuit board, see col. 1 lines 56 – 59. (Claim 3).

The transmit control circuits 302 – 308 of the FRONT END ASIC 30 (Fig. 6) provide signals at the particular selected frequency and at selected delays to the transmit pulsers 202, 204

etc.of the TRANSMIT/RECEIVE ASIC 20 to thereby define a formed beam at a focus. See col. 7 lines 25 – 33. (Claim 4).

Within FRONT END ASIC 30, the FIFO or first in/first out register controls initial delay and then clocked or dynamic delay to shift the focal point on receive whereas weighting for aperture changes occurs via 318 and beam summation at 320. Collectively this constitutes the beamformer stage, see col. 6 line 48 – col. 7 line 18. (Claim 5).

The "sum" of the argument against claim 4 and the argument against claim 5 is that Pflugrath et al effectively teaches both transmit and receive beamforming structure. (Claim 13).

In Pflugrath et al the clocking on the transmit side (CLK to 206) and the receive side (CLK to 214 and also FIFO 312 start and dynamic clocking are all provided from master clock 350. See col. 4 lines 59-63, col. 5 lines 32 – 35, col. 6 lines 54 – 61 and especially col. 8 lines 13 – 23. (Claim 14).

In Pflugrath et al, Analog-to-Digital conversion occurs in 310 of Fig. 6 prior to dynamic focusing; in the final output to display the video signals are converted regardless of output format (NTSC, PAL or RGB color) from digital to analog, see col. 18 lines 8 – 15. (Claim 15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims1, 3-5 and 13 – 15 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Pflugrath et al in view of Knell et al (US6312381, newly of record) further in view of Olson (US5495422) or Langford, II et al. (US5115435), further in view of Wang et al (US6135961, newly of record).

Whereas the anticipatory rejection using Pflugrath et al is predicated upon the Col. 1 line 56 – 59 disclosure that the ASICs 20, 30, 40 and 50 are formed into a single printed circuit board, the obviousness reasoning significantly differs:

In the case of Pflugrath et al alone, col. 6 lines 38 – 41 teaches that with respect to at least the TRANSMIT/RECEIVE ASIC 20, the separate ASICs comprising this member may be combined into a single ASIC and therefore Pflugrath et al exhibits the fundamental recognition that ASICs may themselves be integrated into fewer than their original number.

Since in Knell et al the ASIC-based design includes beamformer 12 as well as transmit timing ASIC 14 providing waveform start signals and the receive beamformer processor 18 and Doppler circuitry include dual PW and CW functionality col. 4 lines 25 – 37, this serves as evidence that all of theT/R, waveform generation, and PW-CW dual Doppler mode functionalities were contemplated as ASIC-implemented in the prior art.

In the case of Pflugrath et al in view ofKnell et al, further in view of Olson, Pflugrath et al in the aforementioned col. 1 and 6 passages as well as Knell et al are assumed for purposes of this argument to fall short of suggesting fabrication of a single ASIC for all of the claim 1 recited functions. However it would have been obvious in view of Olson, see Face Figure, col. 1 lines 27 – 58, col. 2 lines 6 – 11 and col. 16 line 37 – col. 17 line 51. to fabricate a generic ASIC covering a severality of functionalities [in their example case the CDU, MAU and MDU serve as

a logic operation set of three functional circuit blocks within the gate array IC (ASIC) 300] in order to lower development and manufacturing costs and achieve volume cost benefits of such standardization, and additionally since Wang et al cols. 4 – 5 bridging indicates that the concept of varying degrees of unified integration specifically applies to ASIC implementation designs in this art..

Alternatively stated, the ASIC designer would seek to fabricate a composite ASIC (300) in which Pflugrath et al's 20,30,40 and 50 would be likenable to a 300a-d governed by a super-hierarchy gate 304 of Olson so that unused connector pin regions of individualized ASICs would be avoided and the manufacturing simplified. Each of 20 – 50 of Pflugrath et al would literally be embodied in an ASIC having the functionality of all four with gate 304 governance of how they differentiate in use. The net result would not diminish overall ASIC number however each of 20 – 50 would embody the functionality of all of 20 – 50 with a gate-driven control of differentiation in-place. Otherwise the applicability of Knell et al and Wang et al applies.(Claim 3).

In the case of Pflugrath et al in view of Langford et al, the latter notes in col. 1 lines 15 – 43 that since ASICs improve over VLSI by virtue of combining multiple elemental IC functions in a single device, the tendency towards designing of more complex ASICs as active gates (and pin numbers) increase is performance-driven since the signal shuttle-times in routing through multiple IC chips is then diminished by this functional integration.(Claim 3).

The rejection of the dependent claims based upon features of Pflugrath et al per se otherwise carries forward. (Claims 4-5, 13-15).

Claims 2, 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pflugrath et al in view of Knell et al, further in view of Fazioli et al.(US6527722.

Pflugrath et al in view of Knell et al as noted above pertains to PW Doppler ASIC design and contains the claimed structure includes som CW function. Additionally it does so with an ASIC-based beamformer implementation in front end ASIC 30. With note that applicants' para [0019] apparently implements the combination of a CW and PW Doppler ASIC design by the further addition of ASIC circuitry for PW, and the claim merely requires that both Doppler modalities be present in terms of the beamformer capability, it would have been obvious in view of Fazioli to incorporate a CW ASIC function into Pflugrath et al, since the CW processing 300 of Fazioli is also ASIC-implemented (col. 4 lines 29-30), is an acknowledged broad equivalent therein, see col. 1 line 39 – col. 2 line 52 which requires a separate processing path, and is stated to be incorporable into beamformer systems of differing methodologies, see col. 9 lines 64 – 66.

Hence given that Pflugrath et al incorporate PW Doppler in an ASIC beamformer implementation and Fazioli et al acknowledge PW and CW Doppler as equal rank alternatives with particularizations of implementation, provide a CW Doppler ASIC enactment and invite incorporation into various beamformer methodologies, the offering of an ASIC beamformer design capable of both modalities would appear to be an obvious variant. (Claims 2, 7, 12).

In Fazioli the local oscillator 232 is fed to mixer 302 to convert the incoming RF to intermediate frequency IF. Thereafter LO input feeds on 318, 322 to quadrature mixers 314, 316 act on the in-phase and quadrature channels to produce the baseband signal on outputs 324, 326,

see the CW Doppler processor 300 details shown in Fig. 3 and also discussed col. 6 line 56 – col. 7 line 67. Note that either of the LO feed stages is readable against claim 8. (Claims 8. 9).

In the processing contemplated in Fazioli the digitized quadrature outputs of the A/D converted baseband 212a, 212b are left in quadrature for assignment of direction to the bloodflow, see 8 lines 46 – 52. However when a signal intensity or Doppler power is sought then a vector sum magnitude for these sampled signal components must be had, see Pflugrath et al col. 12 lines 35 – 37. Specifically, the CORDIC processor 428 functions as an envelope detector producing the magnitude of the component vectors applied, as discussed in relation to quadrature B-mode, see col. 10 lines 28-37. Thus the aforementioned col. 12 lines 35 – 37 passage analogously operates on the quadrature Doppler signals. Whereas this is PW Doppler, the analogy would extend to CW Doppler after sampling since discrete vector pairs are produced. (Claim 10).

FIR wall filtering 432, flash suppression filtering 434 implemented as min-max morphologic filtering is then practiced on the Cordic-summed baseband data, see col. 12 line 38 – col. 13 bottom. (Claim 11)..

Claims 3, 6 and 13 - 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pflugrath et al in view of Knell et al as applied to claim 3 above except that 'one or more digital signal processors' is now construed as plural, and further in view of Gilling (US6126601), alone or further in view of Olson or Langford, II et al..

Pflugrath et al is silent as to the use of DSPs other than ASIC 40 and therefore does not teach plural DSPs. However it would have been obvious in view of Gilling also directed to a multi-modality (B-mode, Doppler, M-mode) ultrasound beamforming and imaging system to

incorporate more DSP architecture into an ASIC-based system since this allows programming flexibility and ease of update as well as certain lower costs, see col. 2 lines 17-44. Otherwise the 'single ASIC' arguments against Pflugrath et al based upon the aforementioned col. 1 or col. 6 passages apply.

In the alternative the above further arguments regarding multiple functionality transfer onto a single gate-controlled ASIC (Olson) or the argument that applicants are essentially following the art tendency to create more complex single ASICs to improve system performance albeit that a rigidity results in that any re-design must be total in nature (Langford II et al).apply. (Claim 3).

Whereas Pflugrath et al is silent as to M-mode operations, it would have been obvious in view of Gilling for example col. 9 lines 7-19 to incorporate an M-mode along with B-mode and Doppler within an ASIC/DSP implemented ultrasound system since the M-mode like the Doppler spectrograph is a feedout of a single scanline versus time and relatively easily implemented in relation to its diagnostic usefulness such as in characterizing cardiac valve leaflet behavior. (Claim 6).

The applicability of Pflugrath et al against the features of claims 13 – 15 carries forward here by analogy under the Pflugrath et al v Gilling argument base argument. (Claims 13 – 15).

Response to Amendment Arguments

A new ground of rejection is lodged against the combination of T/R and waveform generation and combined PW and CW ASIC claim sets (claims 1 – 2 and newly presented

claims dependent thereon). New grounds of rejection had also been lodged against claim 3 and claims dependent thereon which are centered about the obvious reasonings for single-ASIC implementation for the multiple claimed functionalities. Effectively, Knell et al is being considered as additional evidence that T/R circuitry together with waveform generation circuitry as well as PW-CW Doppler dual functionality were specifically entertained for combined B-mode and Doppler imaging systems, and Wang et al is being considered as additional evidence that large scale integration of ASIC design as taught by the electronics art in general would have applied to such imaging systems in particular.

Any inquiry concerning this communication should be directed to Jaworski Francis J. at telephone number 571-272-4738.

FJJ:fjj

12-26-2005

Francis J. Jaworski
Primary Examiner